

Figure 1

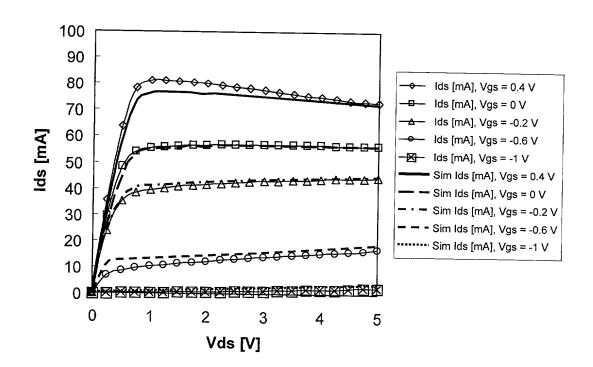


Figure 2

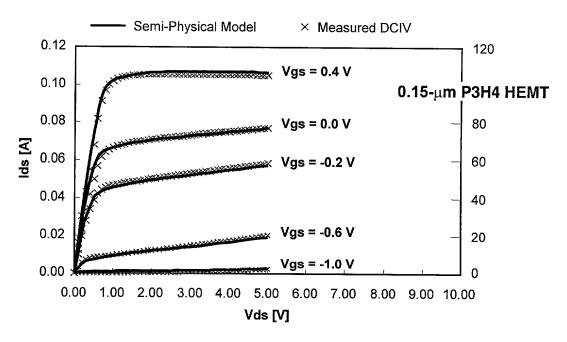


Figure 3

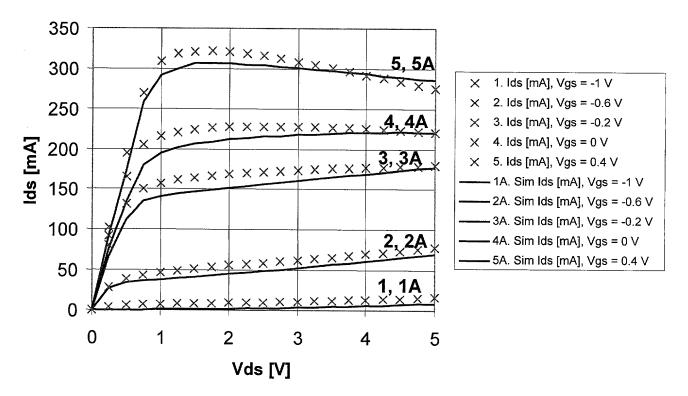


Figure 4

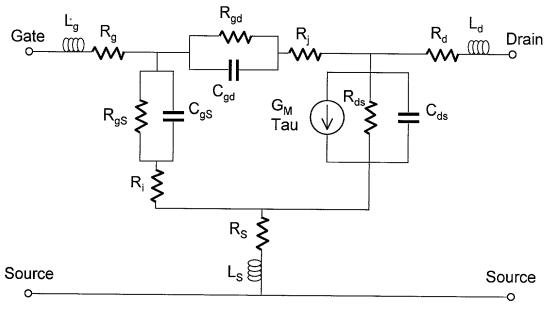


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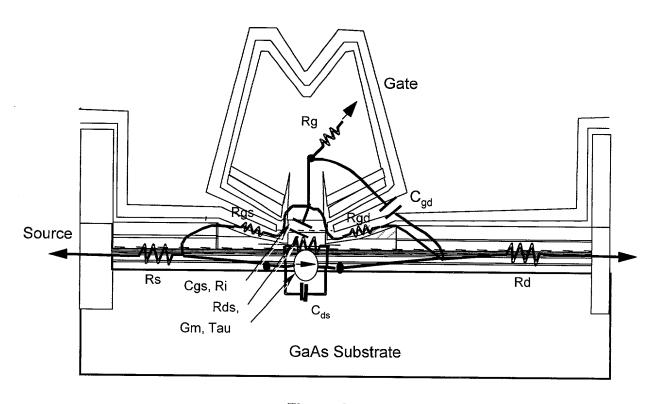


Figure 6

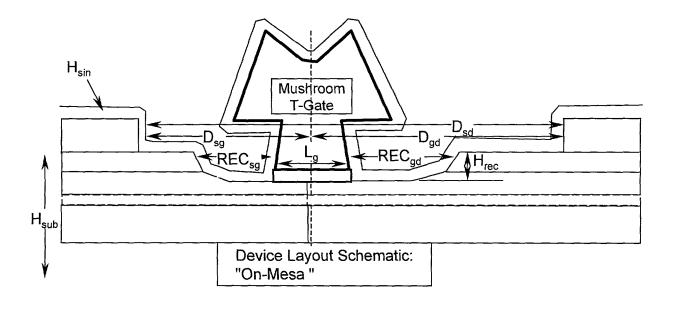


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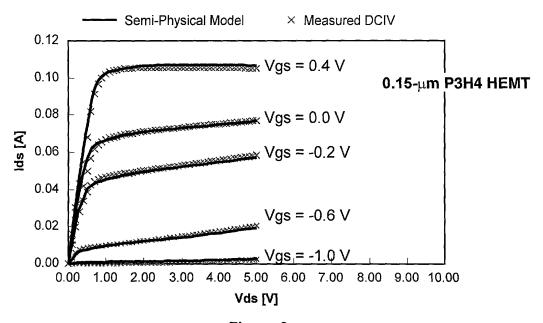


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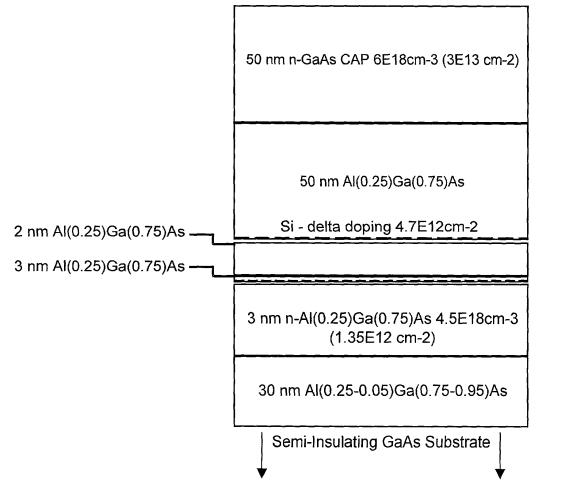


Figure 9

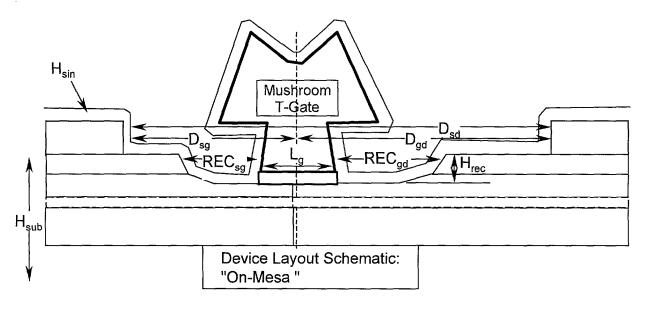


Figure 10

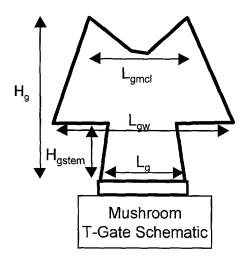


Figure 11

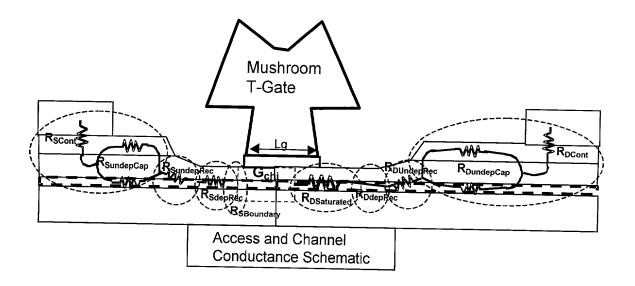
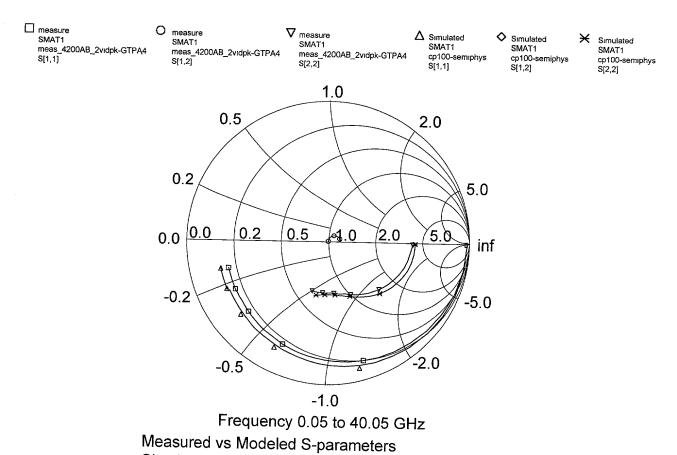


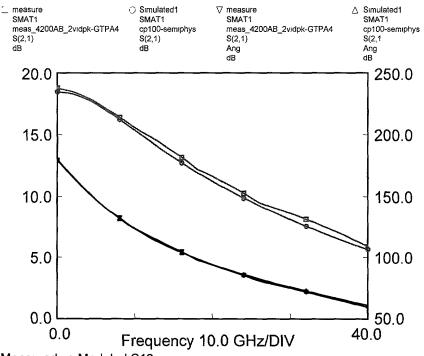
Figure 12



via Semi-Physical HEMT Model

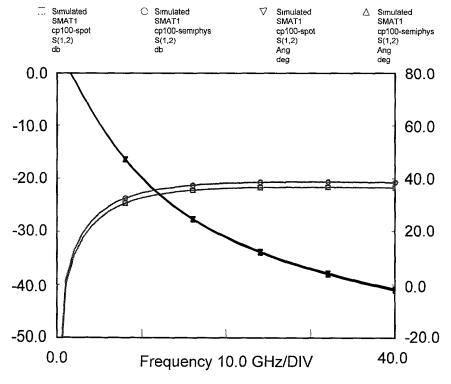
Figure 13

Simulated Equivalent Circuit Element Values



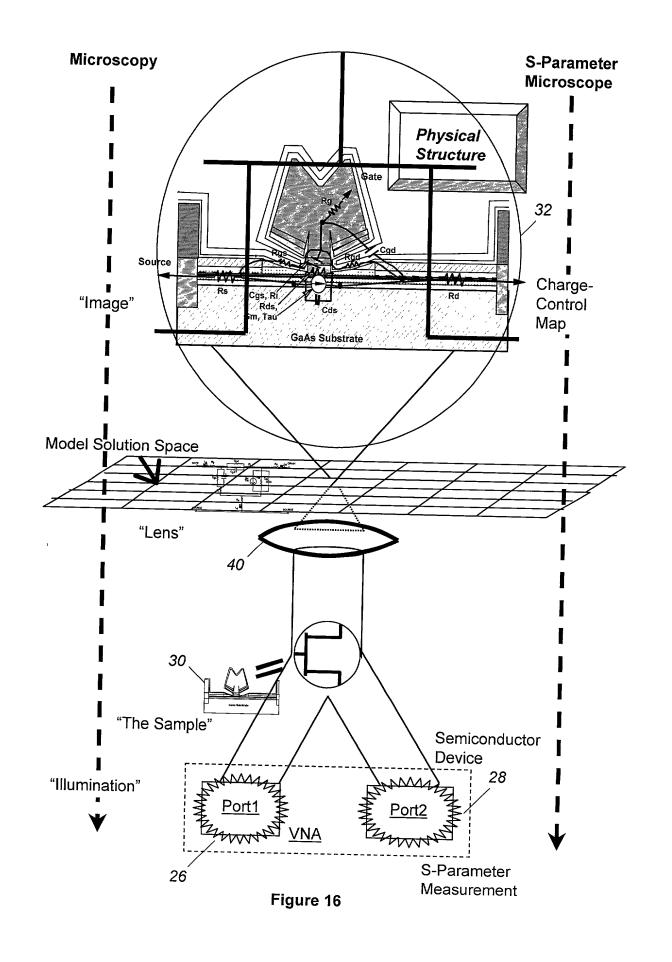
Measured vs Modeled S12 Simulated Equivalent Circuit Element Values via Semi-Physical HEMT Model

Figure 14



Measured vs Modeled S12 Simulated Equivalent Circuit Element Values via Semi-Physical HEMT Model

Figure 15



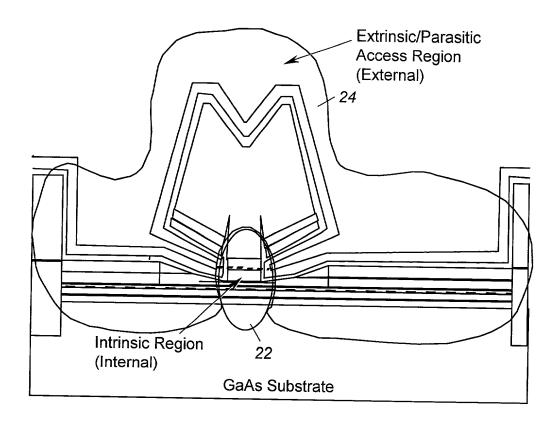


Figure 17

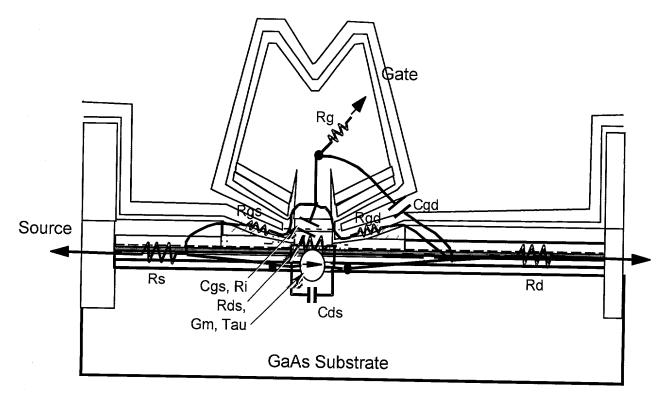


Figure 18

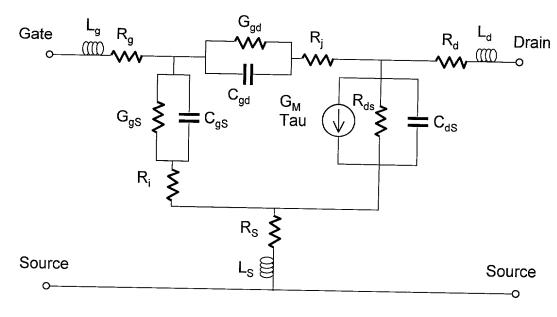


Figure 19

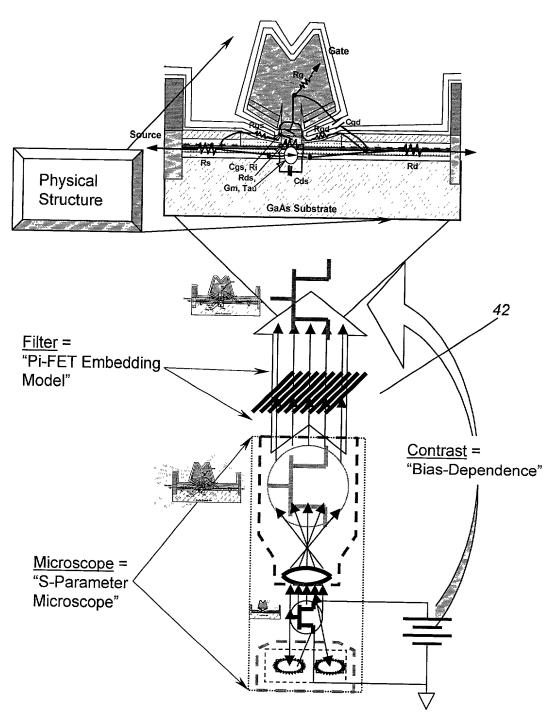


Figure 20

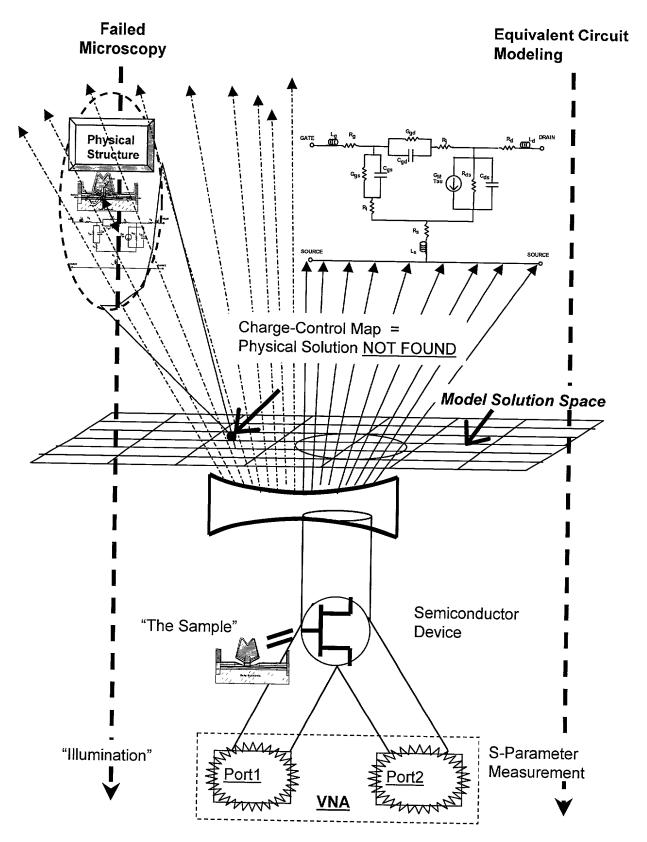


Figure 21

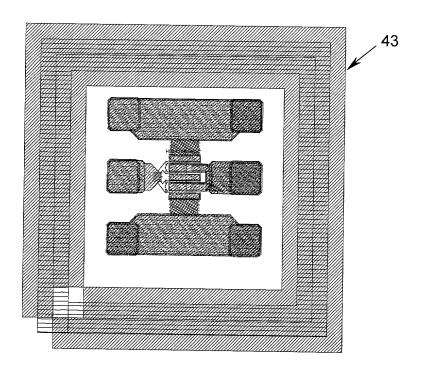


Figure 22

Ids vs Vds for the Measured HEMT Device

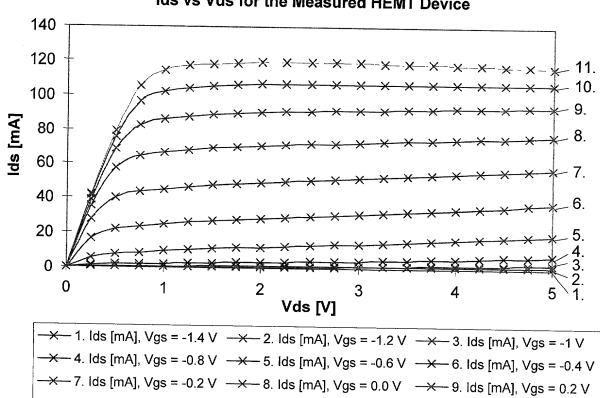


Figure 23

 \rightarrow 10. Ids [mA], Vgs = 0.4 V \rightarrow 11. Ids [mA], Vgs = 0.6 V

lds and Gm vs Vgs for the Measured Device

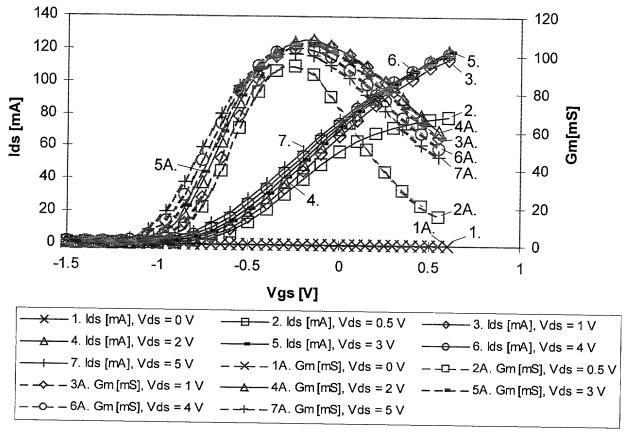
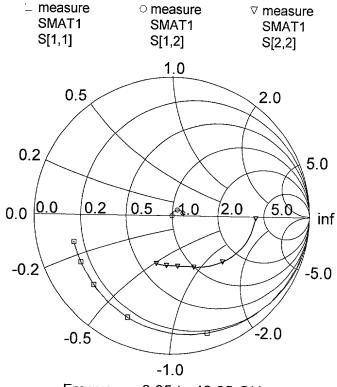


Figure 24



Frequency 0.05 to 40.05 GHz

Figure 25

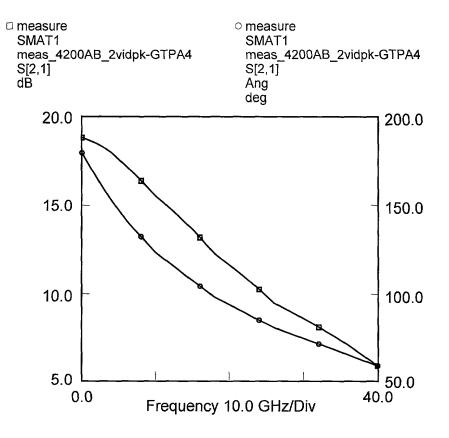


Figure 26

Intrinsic Device Source Resistance vs Gate Bias 0.15 µm P3H4 HEMT

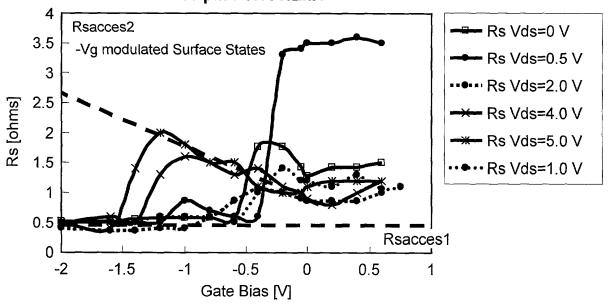


Figure 27

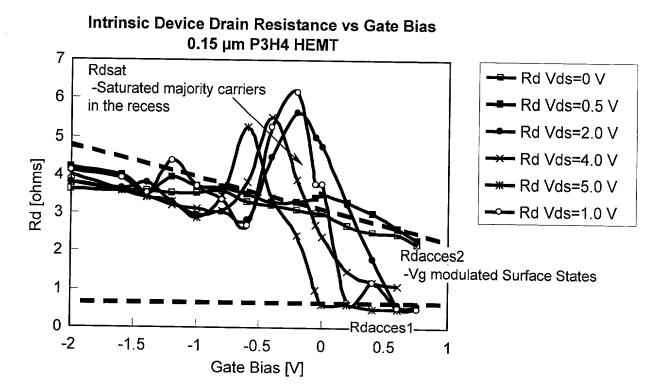
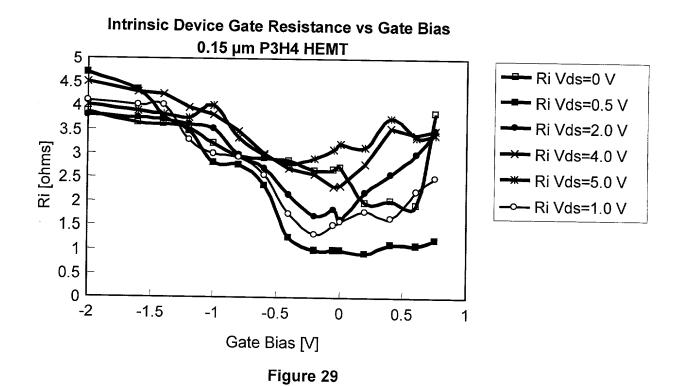


Figure 28



Intrinsic Device Line Capacitance vs Gate Bias 0.15µm P3H4 HEMT

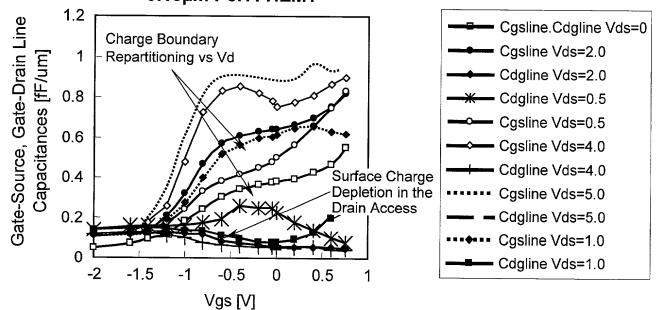


Figure 30

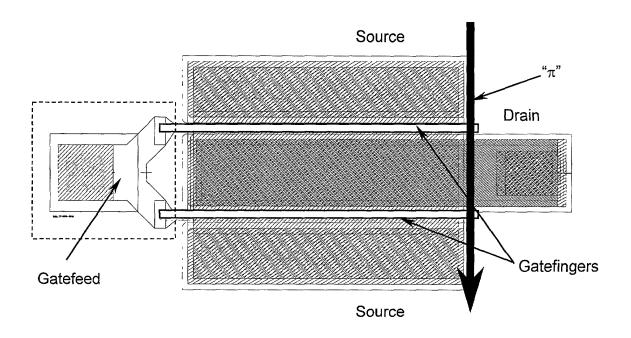


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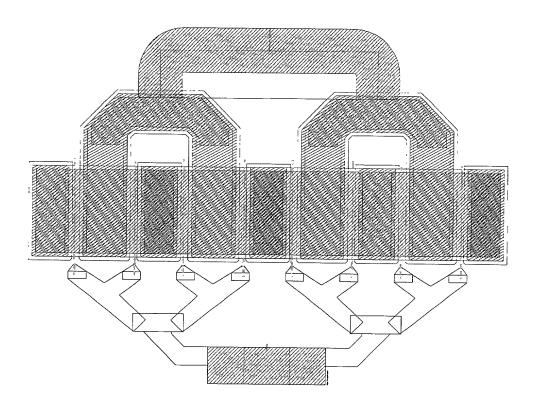


Figure 32

Model Construction

- Off-Mesa, or Boundary Parasitic Model
 Inter-electrode Parasitic Model
 On-Mesa Parasitic Model
 Intrinsic Model

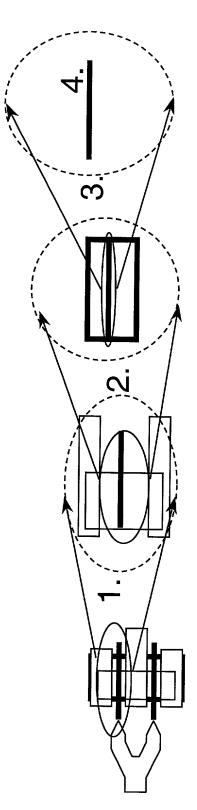


Figure 33

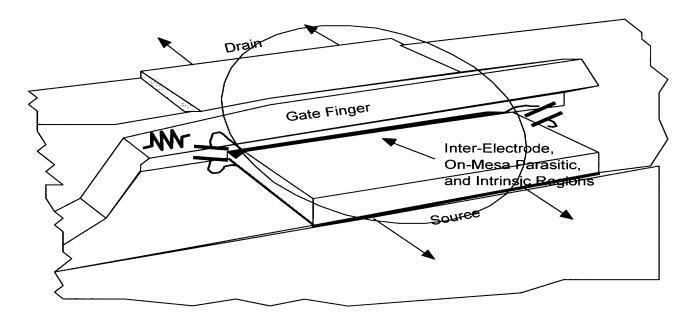


Figure 34

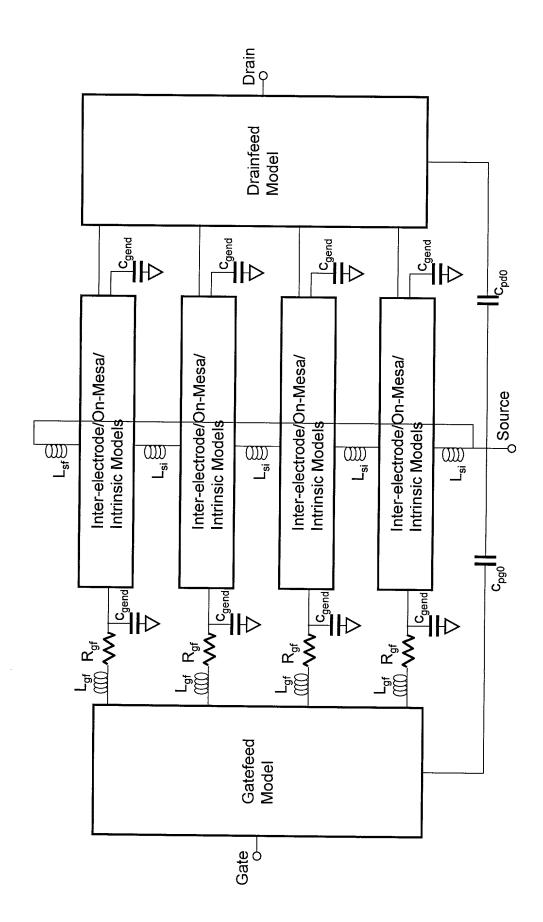


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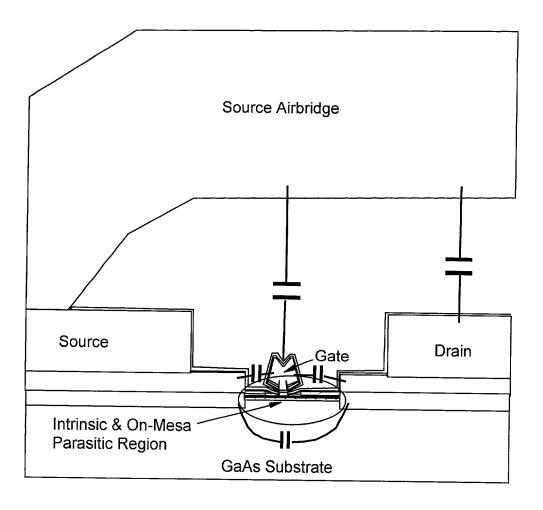


Figure 36

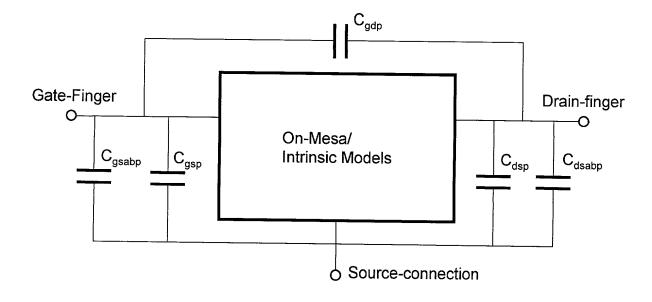


Figure 37

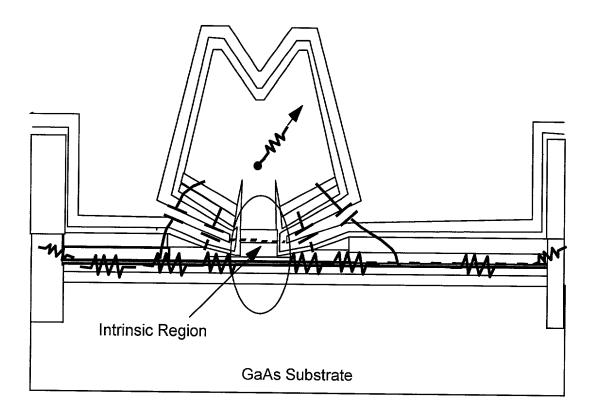


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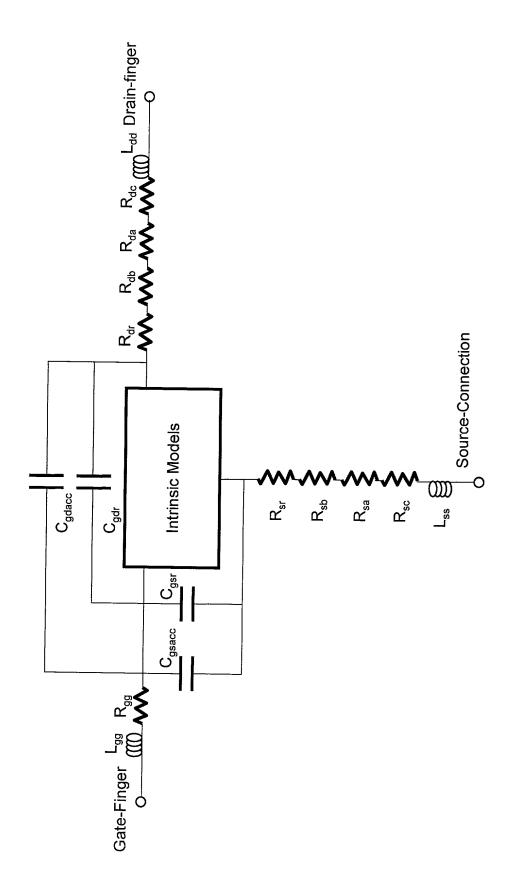


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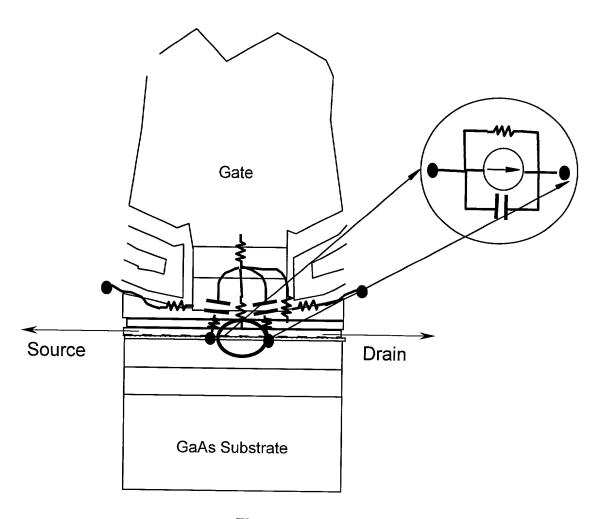


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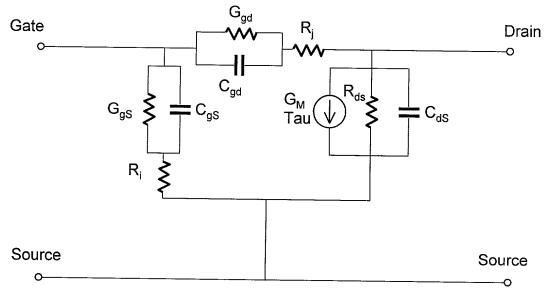


Figure 41

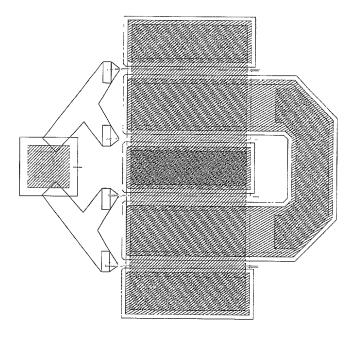


Figure 42A

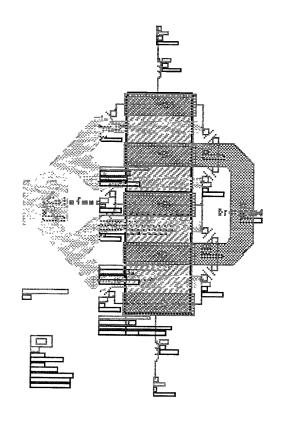


Figure 42B

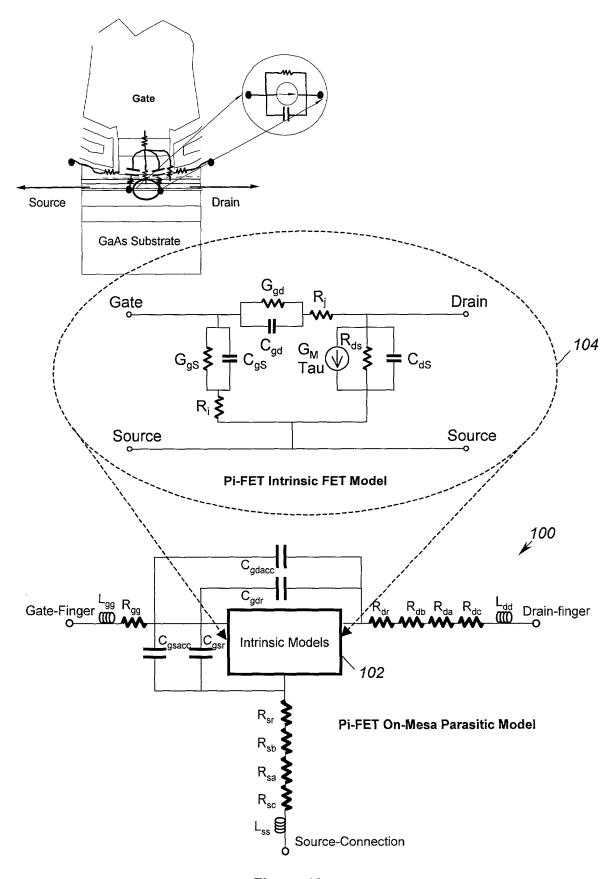


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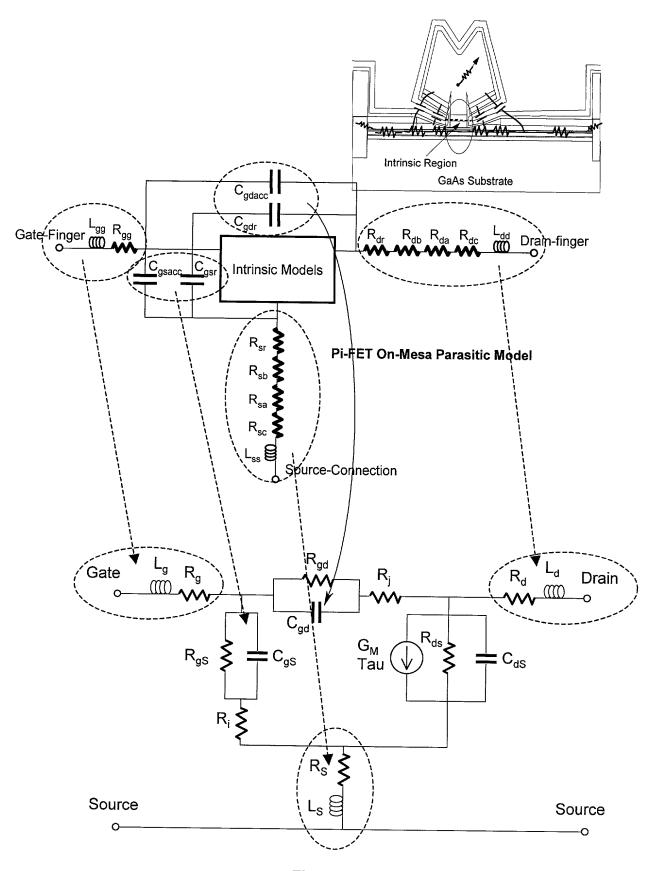


Figure 44

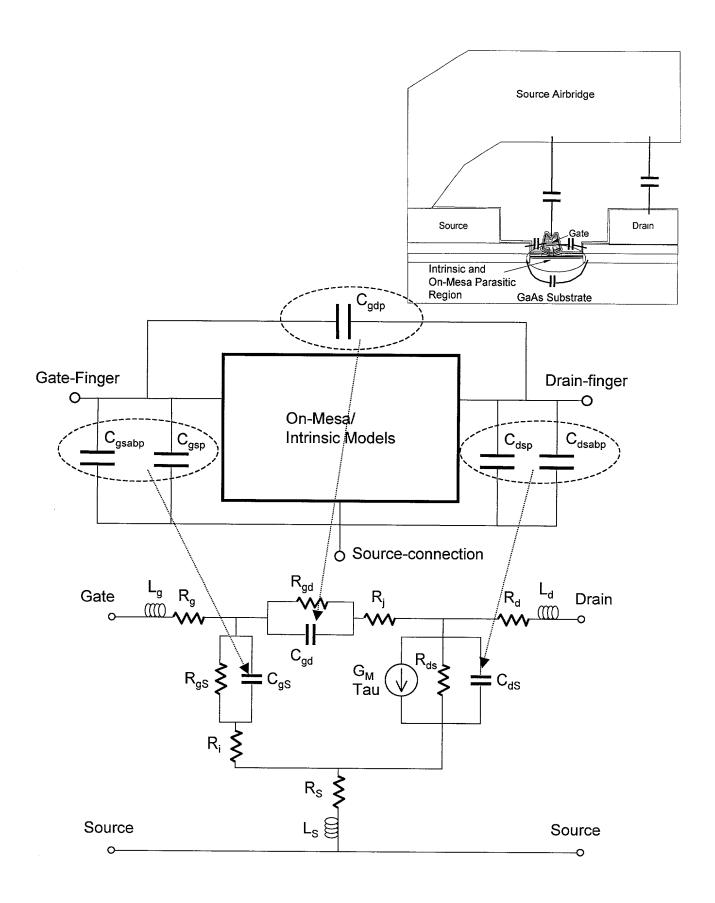


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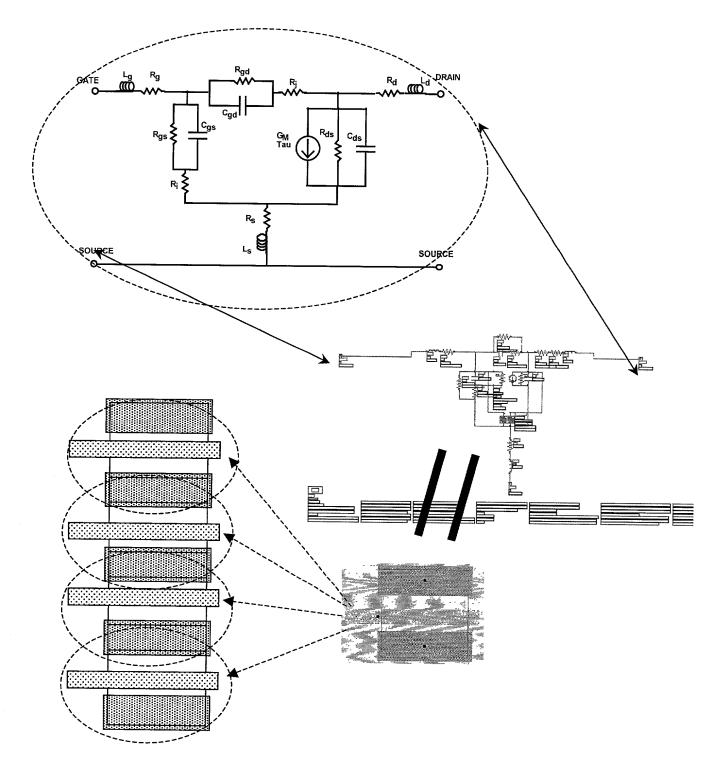


Figure 46

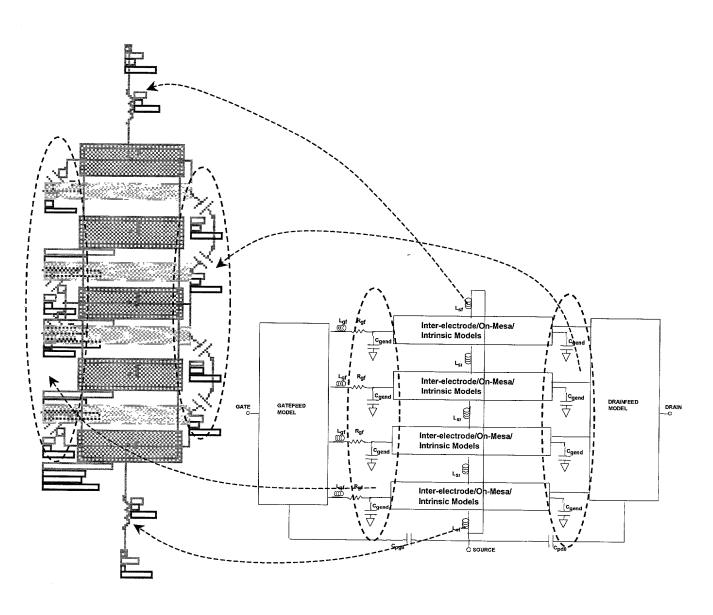


Figure 47

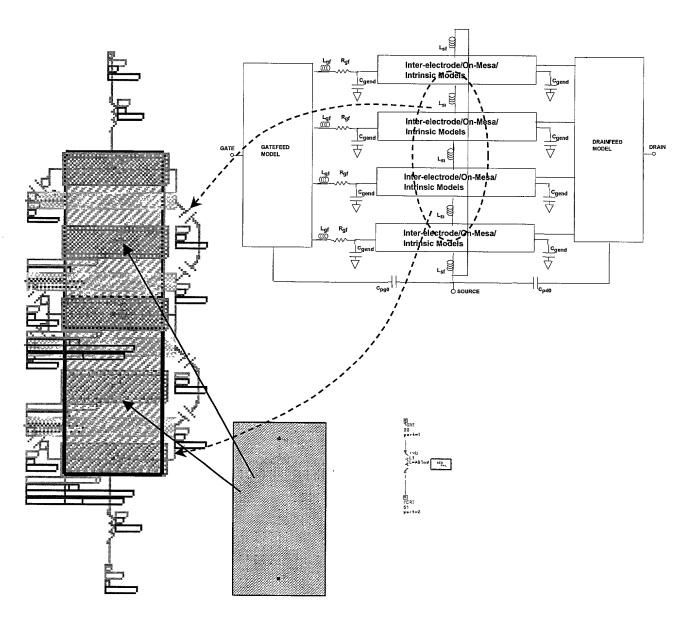
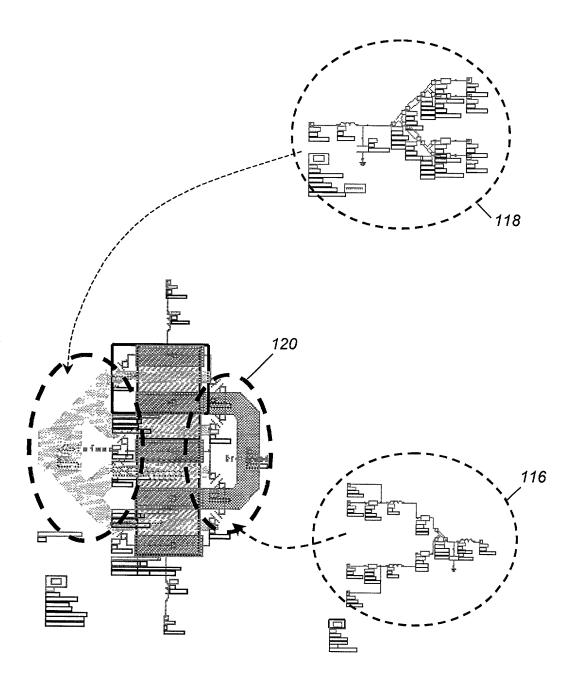


Figure 48



Implementation of the fifth level of embedding

Figure 49

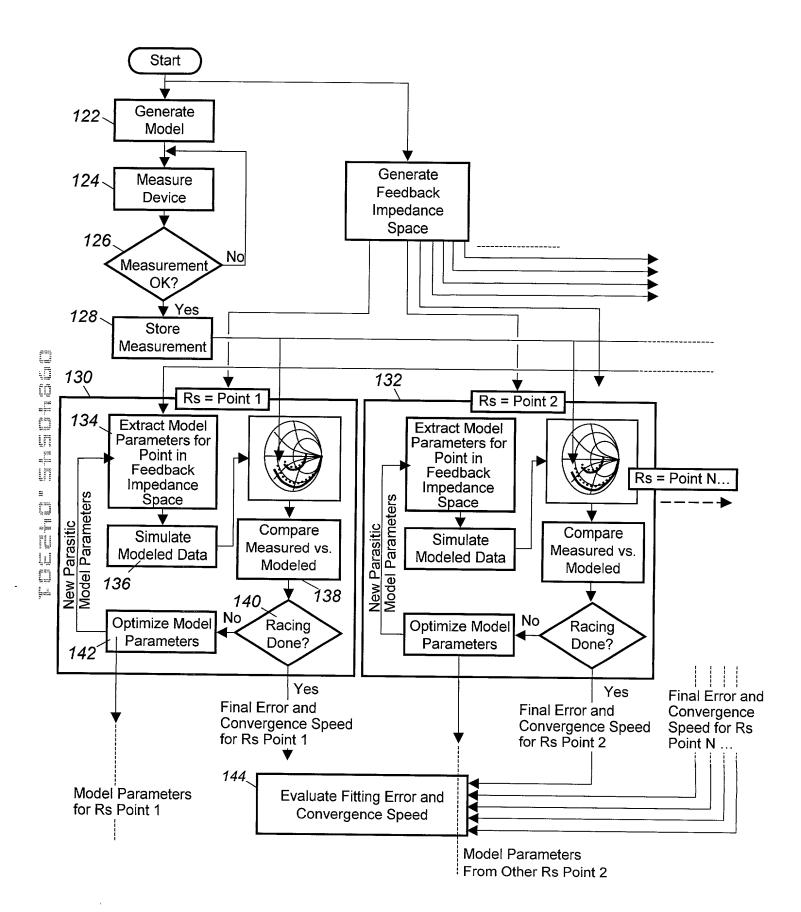


Figure 50A

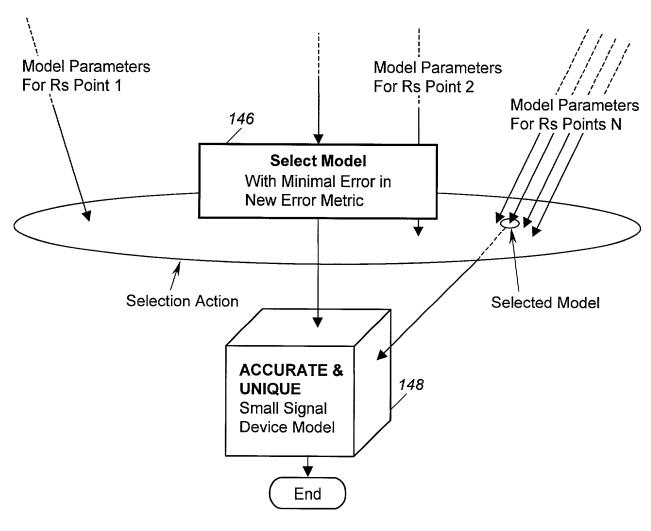


Figure 50B

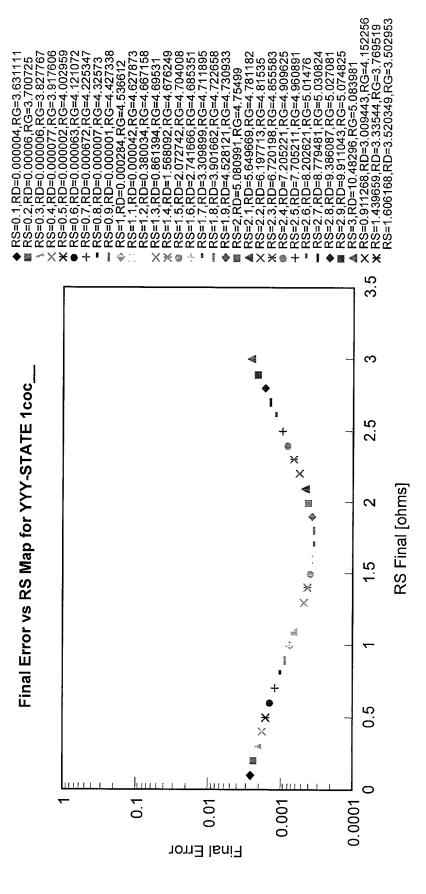


Figure 51

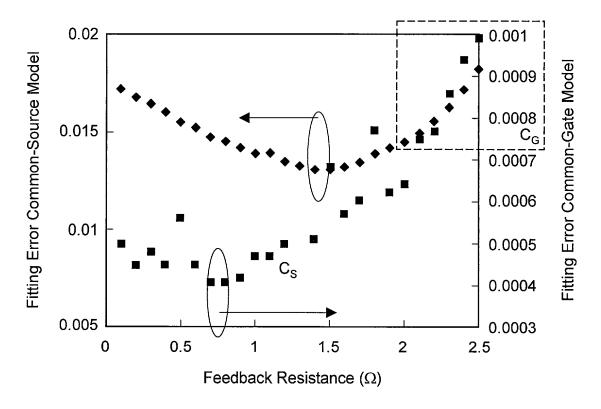


Figure 52

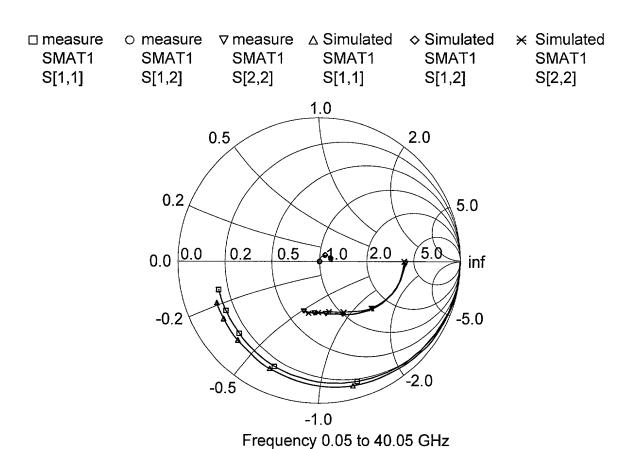


Figure 53A

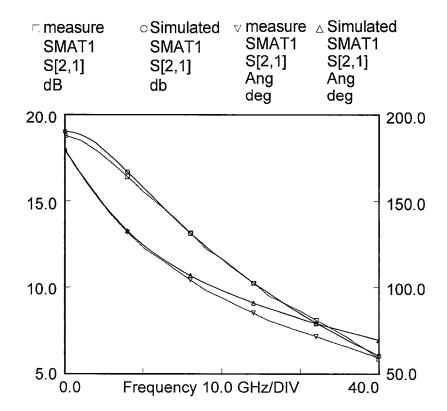


Figure 53B

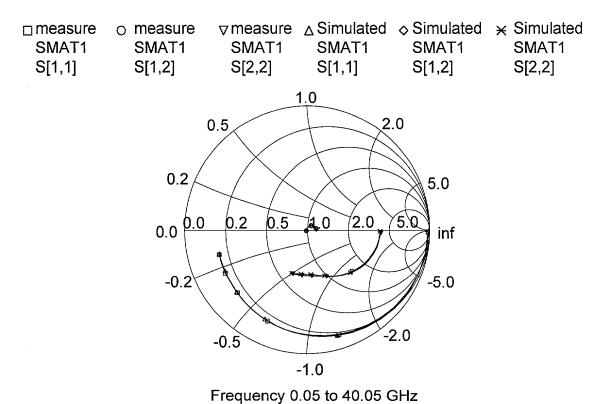


Figure 54A

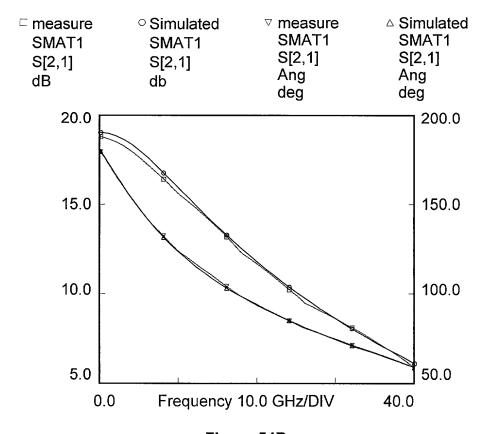


Figure 54B

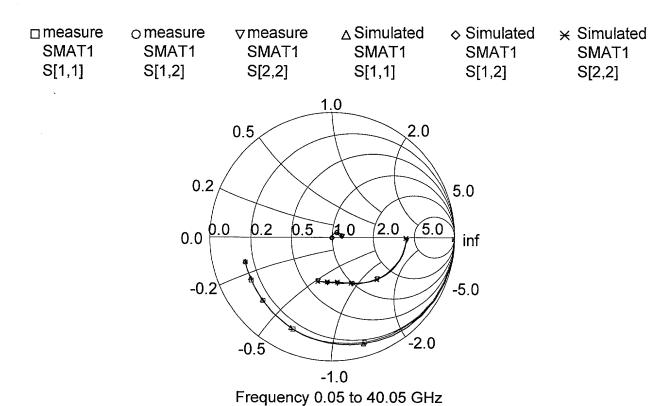


Figure 55A

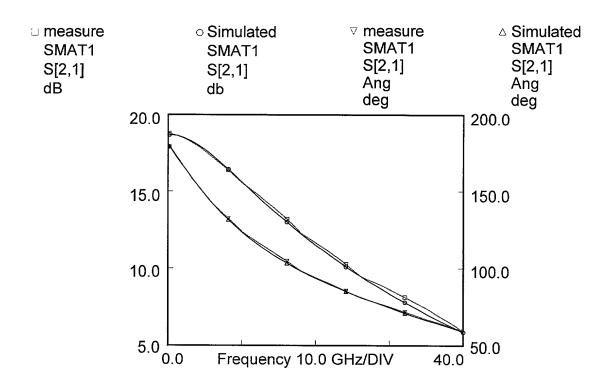


Figure 55B

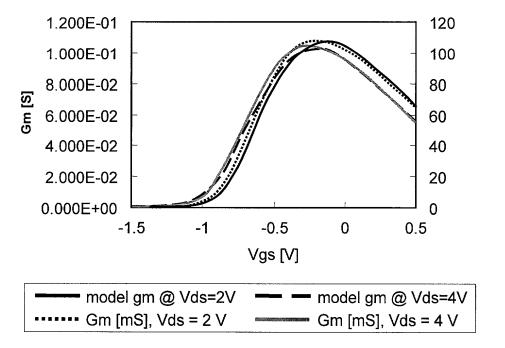


Figure 56

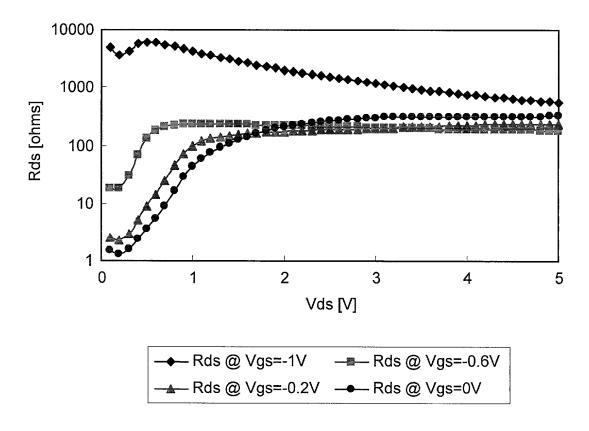


Figure 57

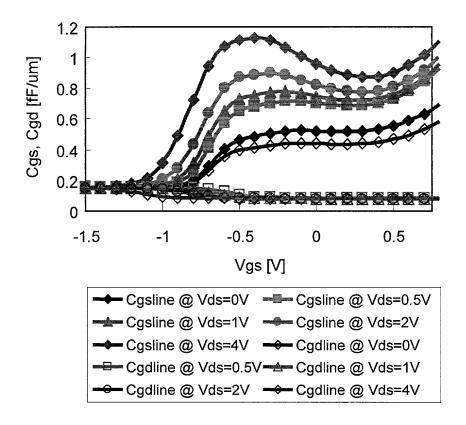


Figure 58

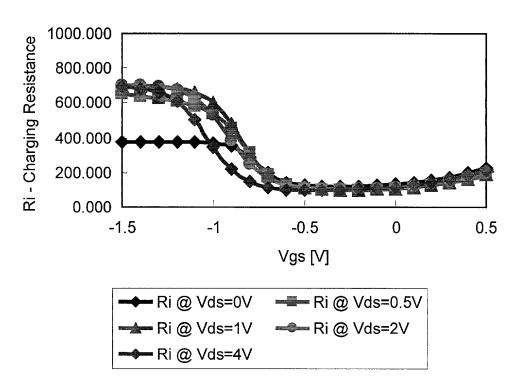


Figure 59

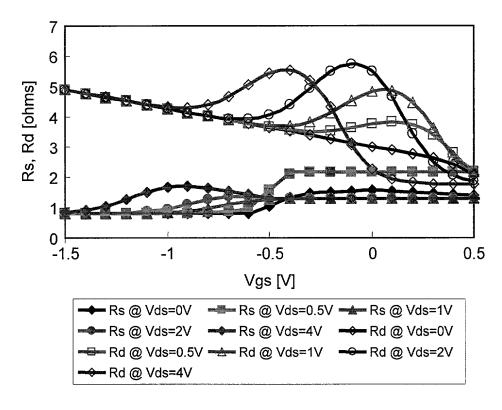


Figure 60

Measured vs Simulated Bias- Dependent Gain @ 23.5 GHz

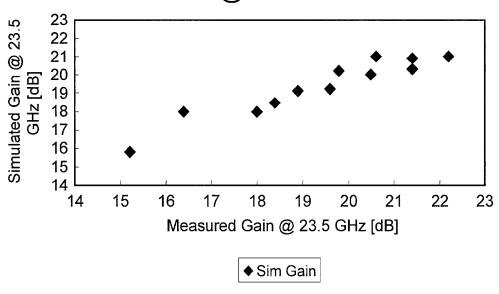
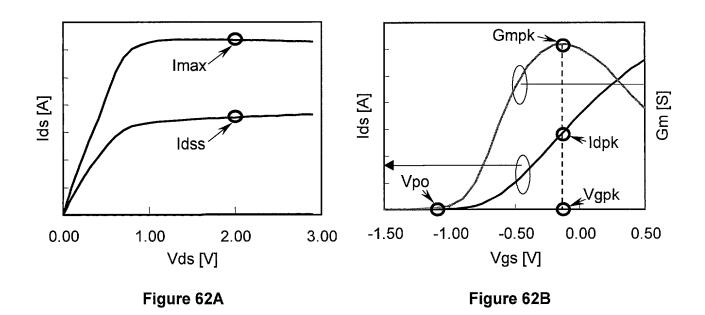


Figure 61



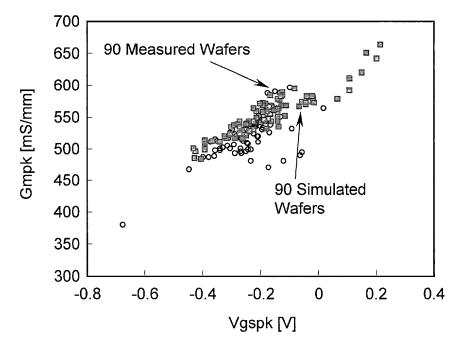


Figure 63

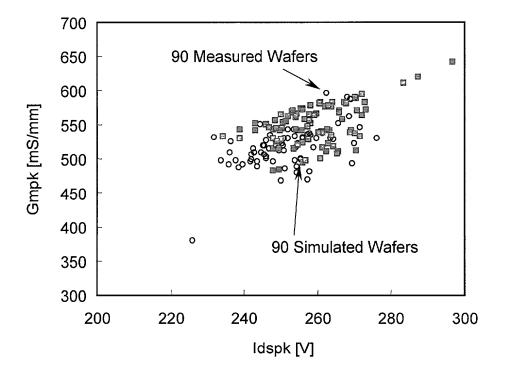


Figure 64

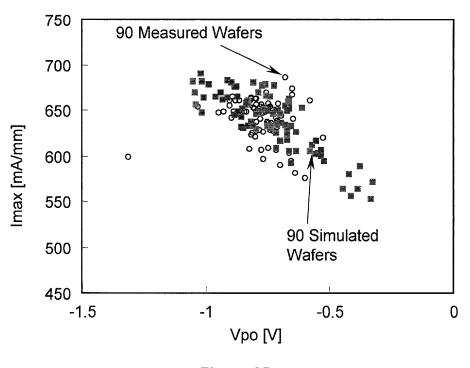
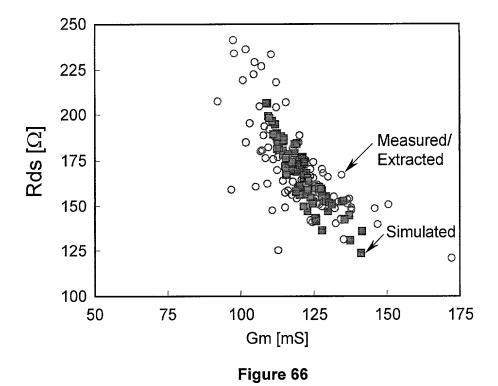


Figure 65



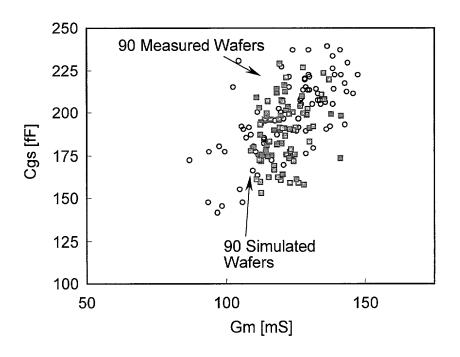


Figure 67

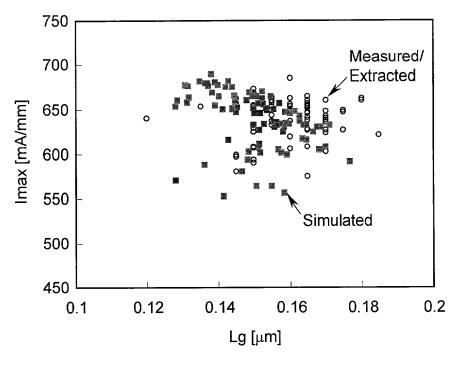


Figure 68

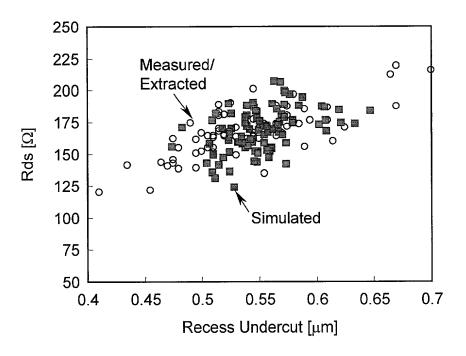


Figure 69